SINO WEALTH

SH6578

Education Computer Module

Features

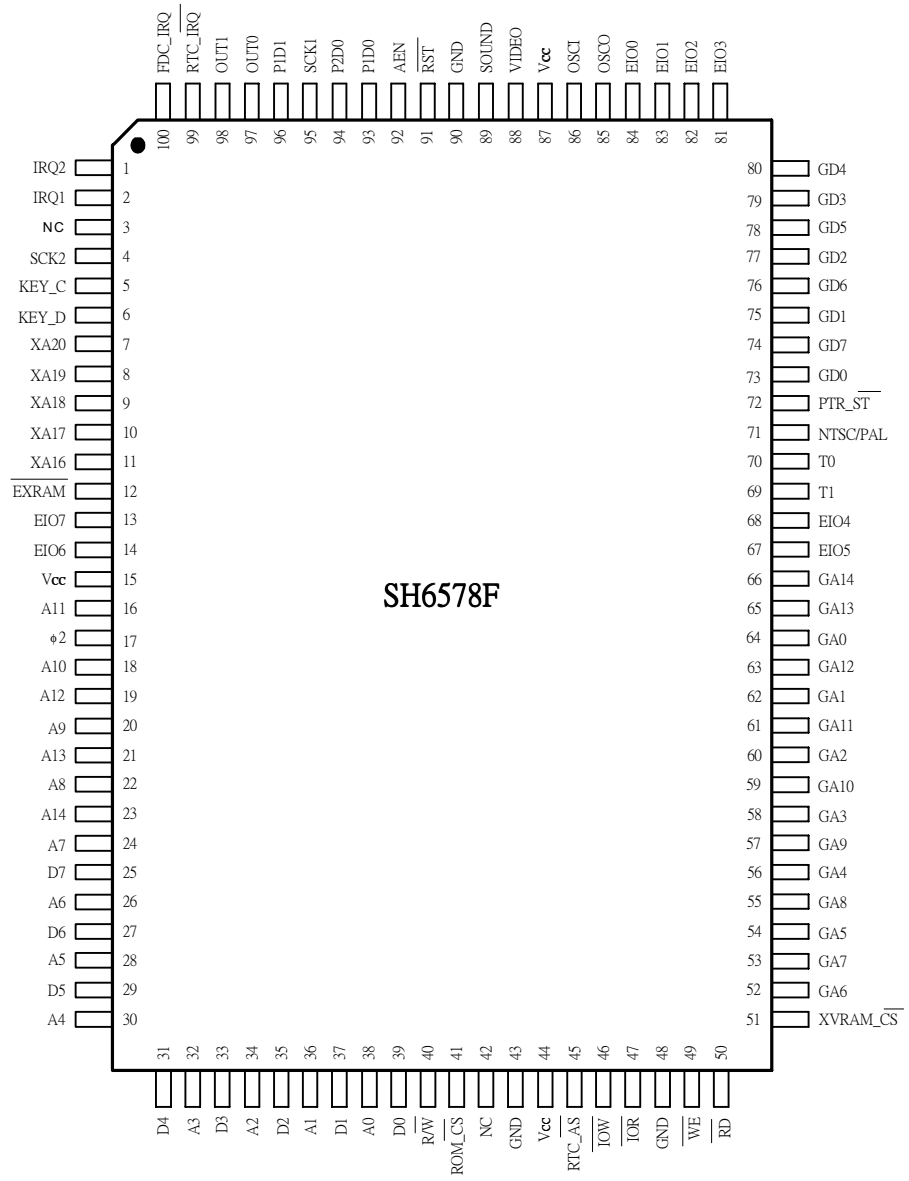
- System
  - CPU: 6502 (1.78MHz)
  - Working RAM: 10K Bytes
  - Video RAM: 10K Bytes
  - DMA
  - Multiple control of IRQ
  - Programmable timer
  - Bank decoder for expandable memory to 1MB
  - T.V. signal output (NTSC, PAL)
- Peripheral Applications
  - Keyboard
  - Joystick
  - Mouse
  - Printer
  - Floppy Disk
- Graphic Processor
  - One 4 page font layer
  - Programmable display area
  - Selectable 4 color or 16 color mode for each font (Both two modes show 53 colors in one frame)
  - Resolution: 256 X 240 pixels
  - 64 color palettes out of 53 display colors
  - 64 sprites in one frame
- Sound Generator
  - 3 programmable channels for sound generator
  - One noise channel
  - One voice channel

General Description

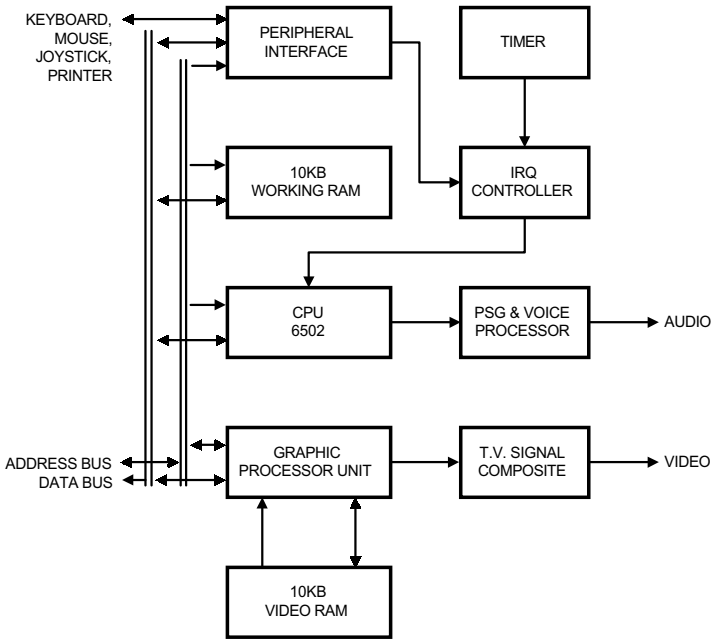
SH6578 is a complete entertainment and education processor. It integrates a 6502 CPU, system control logic, graphic processor unit, programmable sound generator, 10KB working RAM, 10KB video RAM, and other features. Integrating these components into one IC increases the cost efficiency for manufacturing and testing.

Video: SH6578 supports a 4-page size screen of background graphics. The actual display area can be set by the X and Y coordinate positions. Besides background, it also supports a maximum of 64 sprites per frame which suits for displaying variable cartoon applications. About displaying colors, total of 64 color palettes out of 53 colors can be used.
Audio: SH6578 supports 3 melody channels, one noise generator, and one PCM voice channel.
Peripheral: The IC supports many kinds of interface CKT, including keyboard, joystick, mouse, and printer.

Pin Configuration



Block Diagram



Pin Description

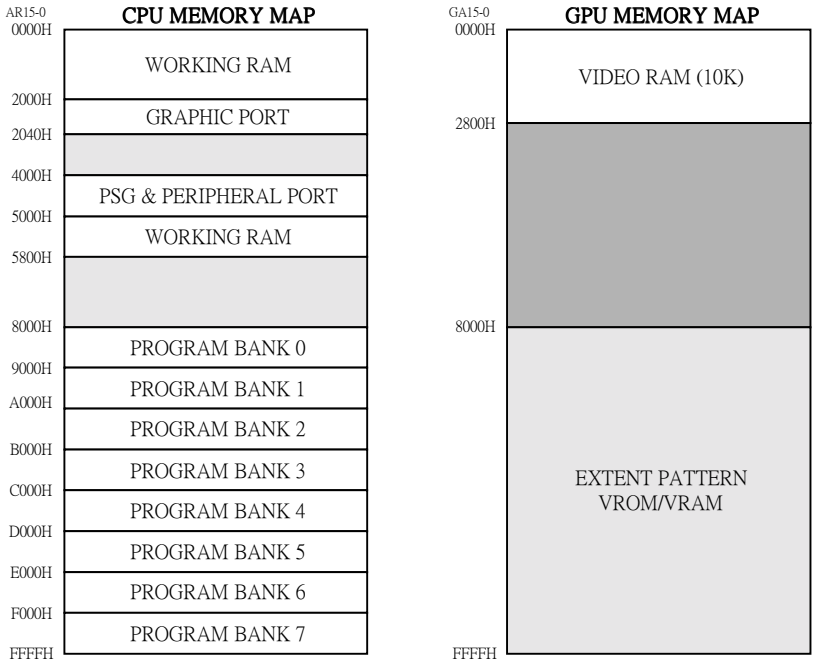
Pin No.	Symbol	I/O	Description
1, 2, 100, 99	IRQ1, IRQ2, FDC_IRQ, RTC_$\overline{\text{IRQ}}$	I	Interrupt request of external signal (IRQ1, IRQ2 and FDC_IRQ are going_high active, RTC_IRQ is going-low active)
95, 4	SCK1, SCK2	O	Clock signal for Joystick 1 & 2
5	KEY_C	I	Connect with AT keyboard clock
6	KEY_D	I	Connect with AT keyboard data
7 - 11, 16, 18 - 24, 26, 28, 30, 32, 34, 36, 38	XA20 - XA16 A0 - A14	O	Address bus of extention Address bus of CPU
12	$\overline{\text{EXRAM}}$	O	For external working RAM ($6000 - $7FFF)
17	ϕ2	O	ϕ2 signal of 6502 CPU
25, 27, 29, 31, 33, 35, 37, 39	D0 - D7	I/O	Data bus of CPU

Pin Description (continued)

Pin No.	Symbol	I/O	Description
40	R/$\overline{W}$	O	R/$\overline{W}$ signal of 6502 CPU
41	ROM_$\overline{CS}$	O	Chip select signal program ROM ($8000H - $FFFFH, 15*)
45	RTC_$\overline{AS}$	O	Signal of address strobe for RTC
46	$\overline{IOW}$	O	$\overline{IOW}$ signal for connecting peripheral (4080H - 43XXH)
47	$\overline{IOR}$	O	$\overline{IOR}$ signal for connecting peripheral (4080H - 43XXH)
49	$\overline{WE}$	O	Write signal for Video RAM
50	$\overline{RD}$	O	Read signal for Video RAM
51	XVRAM_$\overline{CS}$	O	$\overline{CS}$ signal of external Video RAM ($8000 - $FFFFH of graphic address)
52 - 66	GA0 - GA14	O	Address bus of graphic processor
70, 69	T0, T1	I	Test Pin
71	NTSC/PAL	I	TV system select (Open or GND for PAL system, VCC for NTSC system)
72	PTR_$\overline{ST}$	O	Signal for printer to strobe data
73 - 80	GD0 - GD7	I/O	Data bus of graphic processor
13 - 14, 67 - 68, 81 - 84	EIO0 - EIO7	I/O	Extended I/O ports
85 - 86	OSCI, OSCO	I/O	For crystal oscillator
88	VIDEO	O	Composite signal of video
89	SOUND	O	Audio signal output
91	$\overline{RST}$	I	System reset
92	AEN	O	For extending peripheral, like "AEN" signal of ISA bus of PC ($41XX - $43XX)
93, 96, 94	P1D0, P1D1, P2D0	I	P1D0, P1D1: $4016_D0, _D1 for Joystick P2D0: $4017_D0, for Ms mouse or Joystick 2
97 - 98	OUT0, OUT1	O	$4016_D0, D1: output port for preset signal of Joystick 1 & 2
3, 42	NC	-	No connection
15, 44, 87	V_{cc}	I	Power
43, 48, 90	GND	I	Ground Pins

Functional Description

Address Map of CPU & GPU



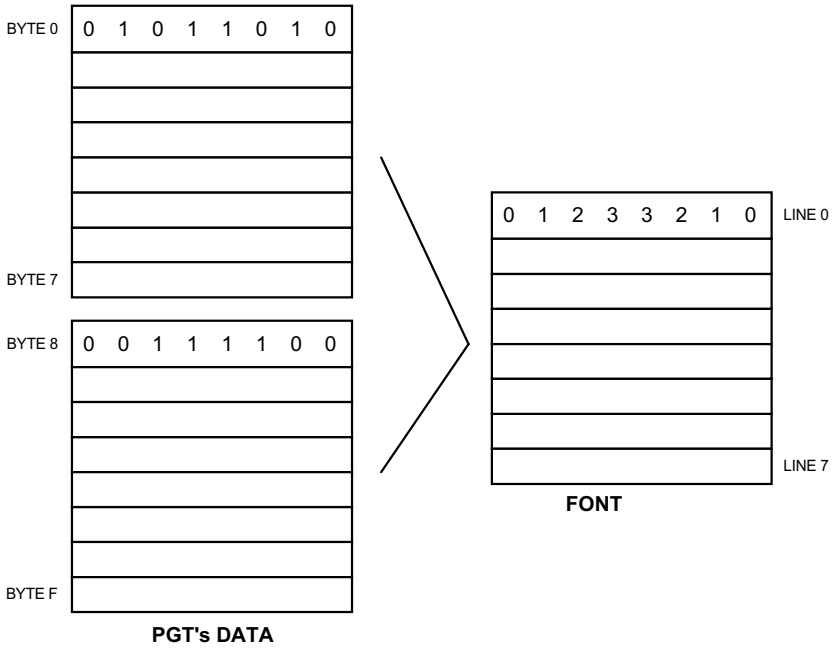
The memory address of working RAM is from $0000H to $2000H and $5000H to $57FFH. The built-in video RAM is from $0000H to $2800H. Although 10KB of working RAM and VRAM were built-in, the maximum access ranges of the CPU and GPU are also up to 64KB. External memory may be appended by using the decoded signals as shown in the application CKT of this system.

Font

Background graphic is composed of fonts. Each font is organized as 8 x 8 pixels. There are 2 color modes: 4 or 16, in which each pixel occupies a different number of bits. (For sprite, only 4-colors can be used for each font and the format is the same as the 4 color mode of background.)

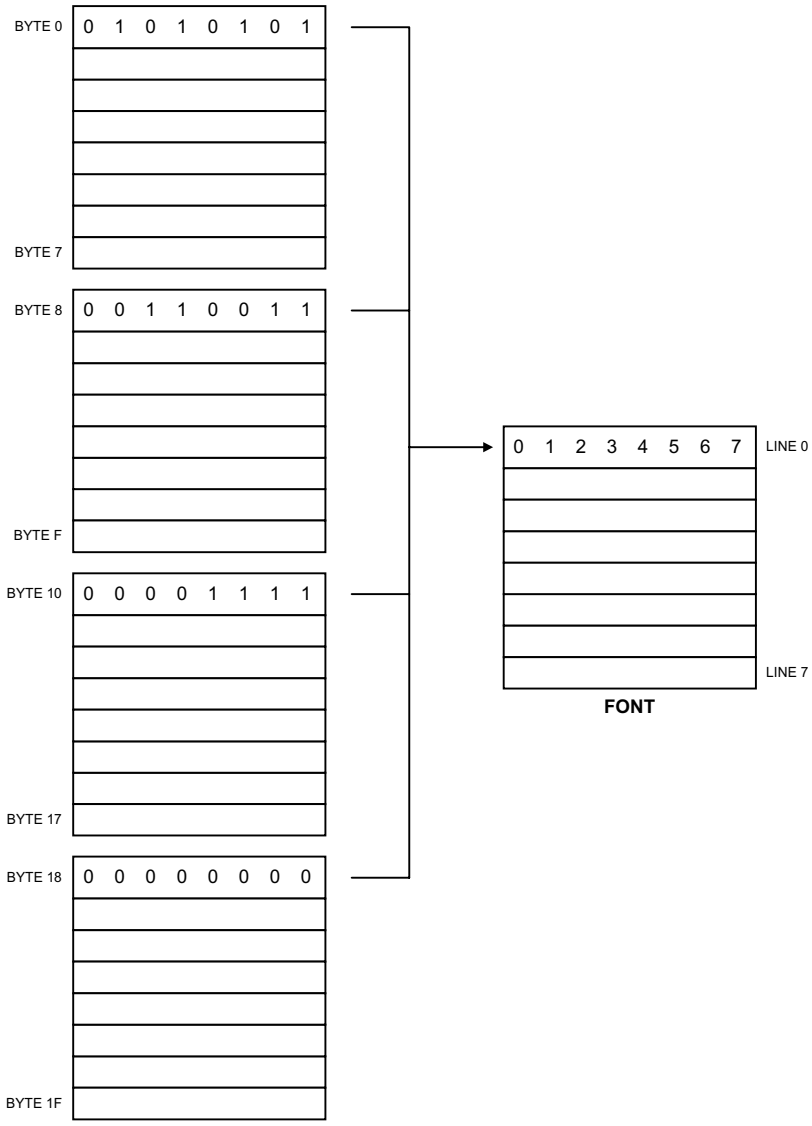
4 Color Mode

In the 4-color mode, each pixel uses 2 bits. Each font occupies 16 bytes of data as follows: 8 X 8 X 2 = 128 bits = 16 bytes. These 16 bytes of data come to the same group as shown below:



16 Color Mode

In the 16-color mode, each pixel uses 4 bits. Each font occupies 32 bytes of data as follows:



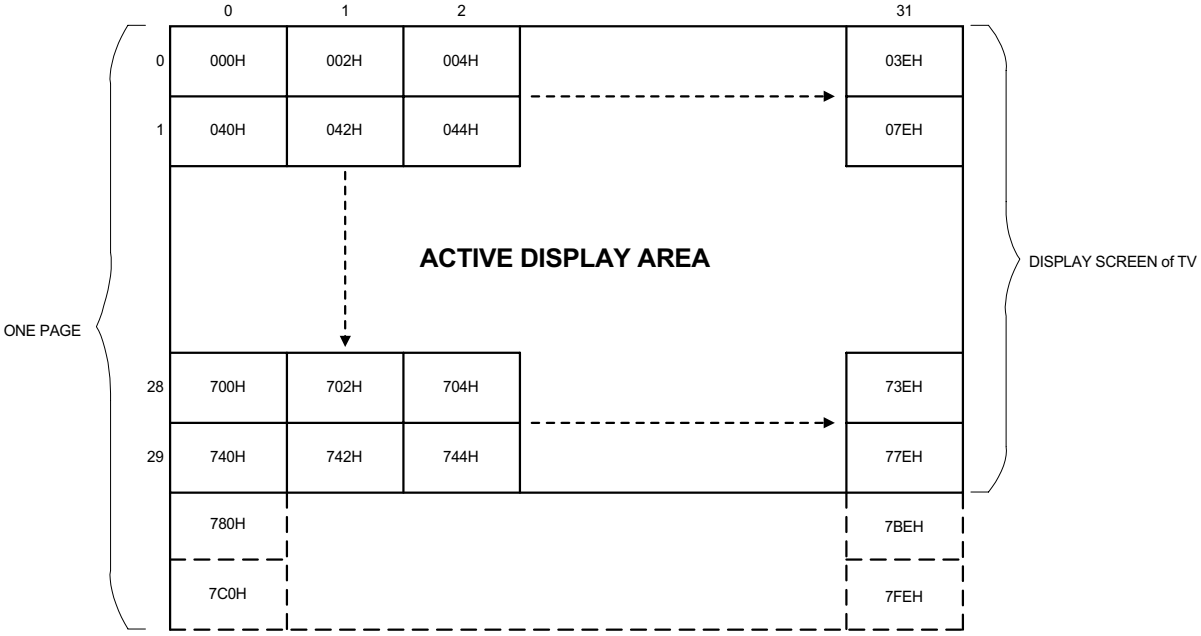
All of the font data was stored in the VRAM. This data is called PGT (Pattern Generator Table). If 64K Bytes VRAM is completely filled with PGT's data, there are 4K or 2K PGTs which can be stored in the VRAM. They are defined by the serial number of every PGT from 0H to FFFH. To call the index of PGT out, the graphic of relation will be shown on the screen. In the 16-color mode, there is a total of 2K PGTs, so the PGT numbers range from 0H to 7FFH.

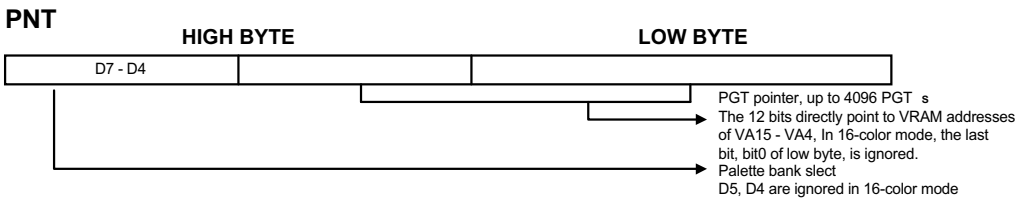
Note:

Although graphic processor can access memory up to 64KB, only 42KB (including 32KB external VARM) are available. So maximum PGT number is Less than above.

Screen

In this system, 256 X 256 pixels are defined for one page graphic which is consisted of 32 X 32 fonts (each font is 8 X 8 pixels). But only 256 X240 pixels are shown on TV screen. The 1024 font indexes called PNT (Pattern Name Table), one page of font, are stored in VRAM. Each PNT occupies two bytes as shown below:





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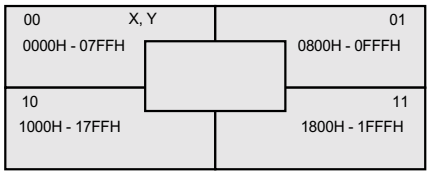
Background Graphics

SH6578 supports 4 pages of display frames which are linked together to form a square. It allows page-selection of $2000H and the setting of X and Y values of $2005H to define the display area.



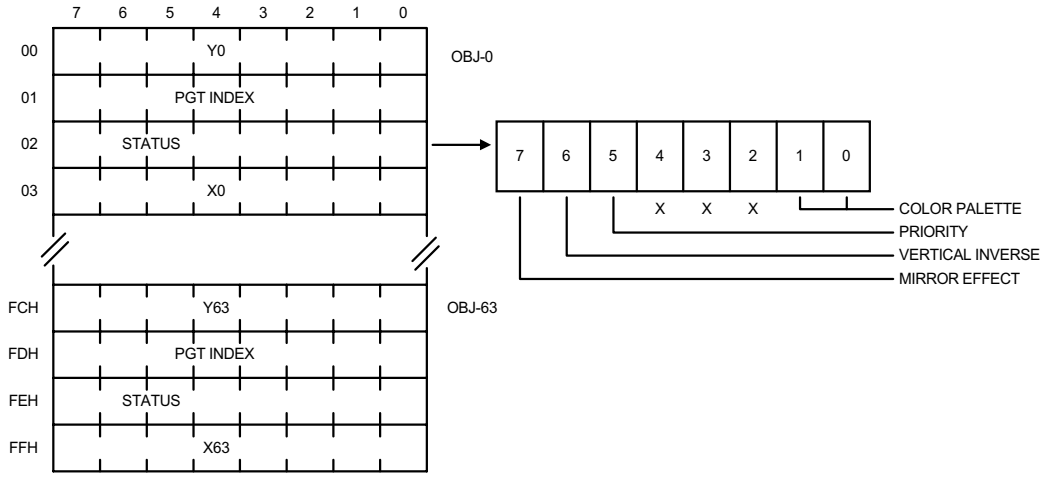
Memory Map of Background Graphics Plane

Sprite

Sprite can be used to display cartoons and characters. Each sprite is composed of 8 x 8 or 8 x 16 pixels and all of the parameters are independent; such as the display position, color palette, and PGT index. SH6578 supports 64 sprites in one frame, making it convenient for the programmer to show some variable cartoons. On these 64 sprites, the lower serial number is defined to higher priority of display. OBJ-0 is the highest priority and OBJ-63 is the lowest. If some sprites overlap, the lower priority one will be covered.
Each sprite has 4 bytes of parameters which is called Sprite-Attribute-Table. Totally, 256 bytes of data were stored. These memories were also integrated in this system, but do not belong to CPU address mapping.

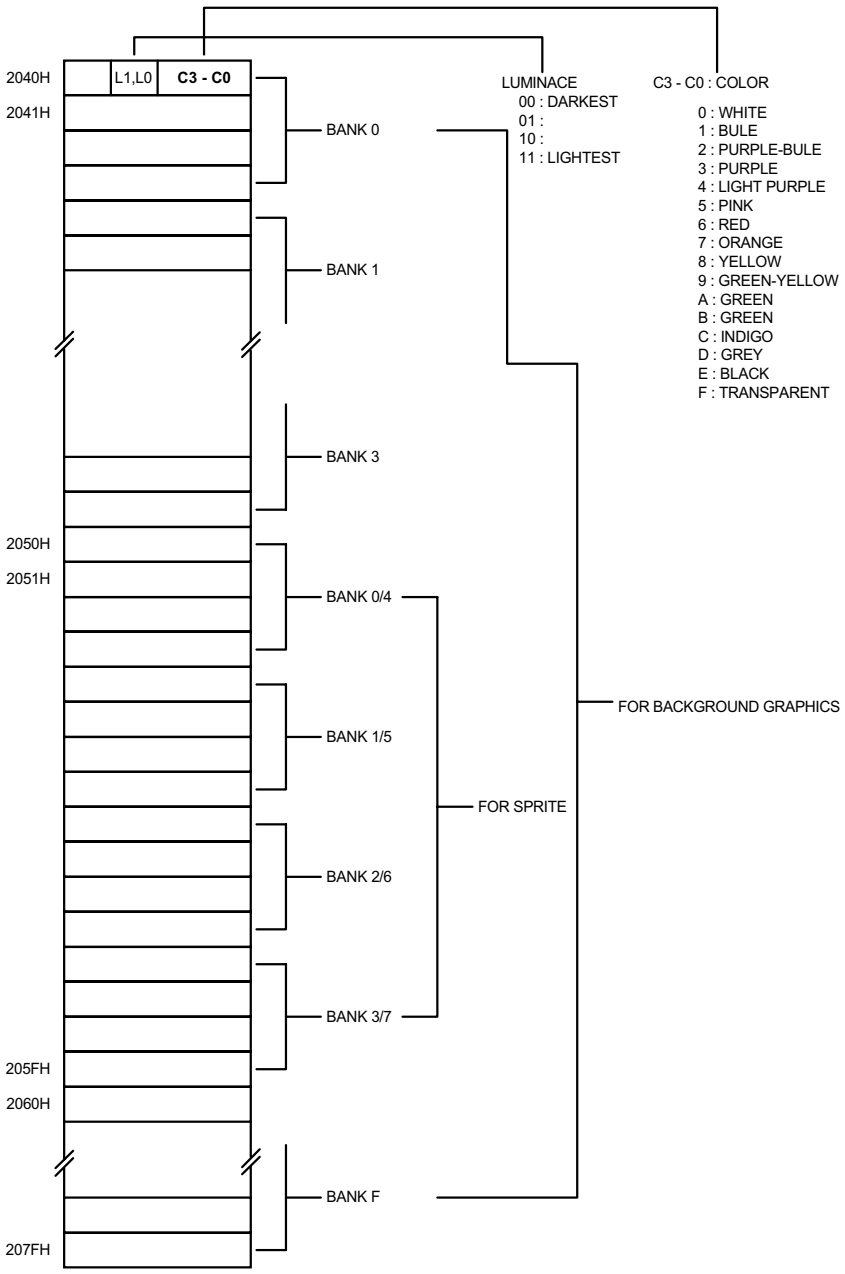
The diagram below is the data format of sprite. The first and fourth byte, Yn and Xn, define the display position of sprite's top-left corner on the screen. The second byte, PGT index, is the PGT name that has the same definition as background graphics, but the 256 PGTs can only be accessed. The third byte, Status, defines the attributes of that sprite. If bit 7 and 6 are set to "1", the display pattern will cause a mirror effect and vertical inverse. Bit 5 is the priority bit, sprite compares with background graphics, setting it to "1" is higher priority. When this sprite overlaps with the background, the lower priority will be covered and the higher one will show on the screen. The definitions of bit 1 and 0, color palette, are same as background graphics, but only 16 colors can be used.

Data Format of Sprite



Note: 256 bytes of memory were included in SH6578, but don't belong to the CPU register. The only way of updating data is through DMA of $4014. The user must put all of data in working RAM, then start DMA.
The user must only use DMA during V_Blank or when GPU is off.

Color Palette (2040H - 207FH)



Note: In the 4-color mode, the 64 color palettes are divided into 16 banks. Each bank includes 4 colors. In the 16-color mode, they are only divided into 4 banks containing 16 colors each.

Register Description

D7 - D0

4031H W INITIAL SETUP

For initial system setup, writing “6576” into $4031h is necessary, and must execute the write-instruction within two instruction cycles.

For example:

```
LDA     #65h
LDX     #76h
STA     INITIAL_SETUP
STX     INITIAL_SETUP
  :
  :
```

7	6	5	4	3	2	1	0
	X		X	X			

2000H W SYSTEM CONTROL

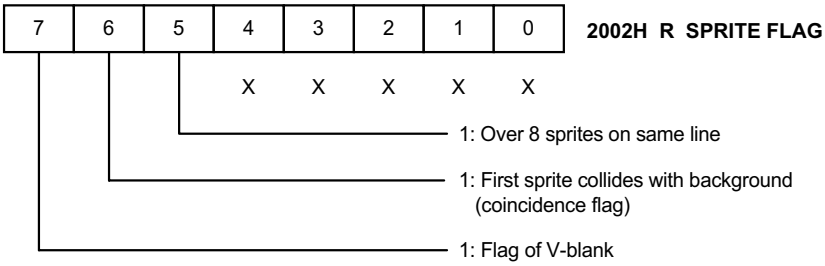
- Bit 1, 0: Page selection of background graphics for screen.
  These two bits set display pages.
  0 0 : Page 0; 1 0 : Page 2;
  0 1 : Page 1; 1 1 : Page 3;
  (Refer to page 12 for detail)
- Bit 2: Increment amount of address counter , refer to $2006, $2007 registers
  0: +1
  1: +32
- Bit 5: Sprite mode
  0: 8*8 pixel mode
  1: 8*16 pixel mode
- Bit 7: NMI enable
  1: enable
  0: disable

"NMI" signal of UM6502 is connected with the signal of the vertical blank. It is a timer or flag of updating data. The user can only update the VRAM data during the vertical blank or when the display is off. (Normally, during the running of program, the screen should not be turned off.)

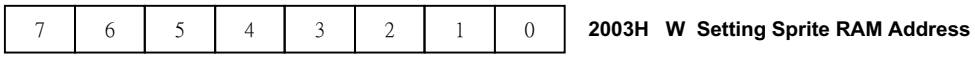
7	6	5	4	3	2	1	0

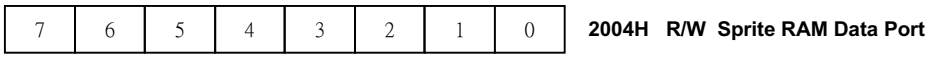
2001H W COLOR & DISPLAY

- Bit 0: Color output control (0:Color output, 1:B/W output)
- Bit 1: Mask display control for Background display
  0: Nonmask, normal display for 256 pixels
  1: mask 8 pixels of background on left side of screen
- Bit 2: Mask control for Sprite display
  0: Nonmask display of Sprites;
  1: The sprites will be masked as locating on the left side 8 pixels c screen
- Bit 3: Background graphics enable (1/0: enable/disable)
- Bit 4: Sprite enable (1/0: enable/disable)
- Bit 5: Blue enhance
- Bit 6: Green enhance
- Bit 7: Red enhance

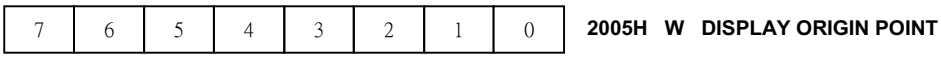


Bit 5 is set to a "1" whenever there are more than 8 sprites on same horizontal line.

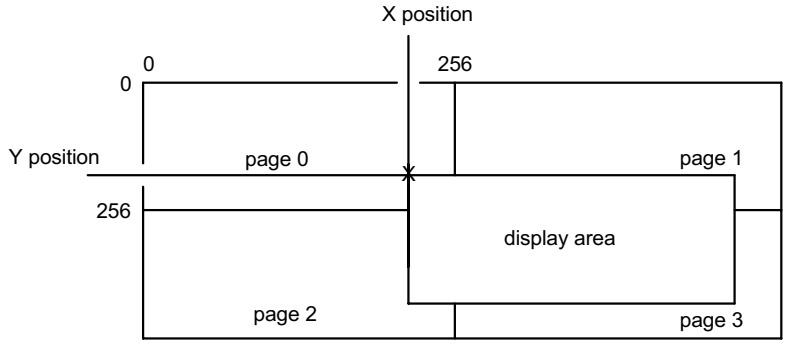




The 256 sprite RAM data, not belong to CPU memory, which normally are updated by DMA also can be accessed by CPU from these ports (CPU can't directly access). User must set address first with writing 8 bits address to $2003h then reads or writes data sequence from/to $2004h.



This register is used for setting the display area of background graphics. In the following diagram, the X, Y values are written to set position, X first then Y by two bytes. For 8-bit value of this register, the maximum is 256 pixels, which should be combined with $2000 -D0, D1 to make a complete value of X, Y coordinates.



D7 - D0	**2006H W VRAM Address**

Setting VRAM address, two bytes set up, high byte first (GA15 - GA8) then low byte (GA7 - GA0).

D7 - D0	**2007H R/W VRAM Data Port**

The bus of CPU and GPU are independent, therefore, the CPU can't directly access VRAM's data. Using these two ports is one way to read or write VRAM's data for CPU. Set address value of VRAM from $2006H first, then read $2007H to get or write data into VRAM from $2007H. When reading or writing $2007H one time, the address counter will increase 1 or 32 automatically.

Note: While reading data, "first-reading" is ignored. The following program is an example for reading or writing data from/into VRAM.

Ex.: read data from VRAM of $2000H and $2001H

```
LDA   #20
LDX   #00
STA   $2006     ; (set VRAM address)
STX   $2006
LDA   $2007     ; (first bytes is ignored)
LDA   $2007     ; (data of $2000.)
LDA   $2007     ; (data of $2001, if $2000_D2 is set to 0)
```

D7		D3, D2		D0	**2008H R/W Color Select & PNT Start Address**

- D0 → Start address of background graphics PNT Table
  D0 = GA13 (GA14, GA15 = 0)
  (Note : if D0=1, that means PNT table is ranged from $2000h, so only $2000h~$27FFh VRAM is avtiable for PNT, that means only one page can displayed on TV screen)
- D3, D2 → Start address of sprite PGT Table
  D3, D2 = GA13, GA12 (GA14, GA15 = 0)
- D7 → Color mode of background graphics
  0: 4 colors of each font
  1: 16 colors of each font

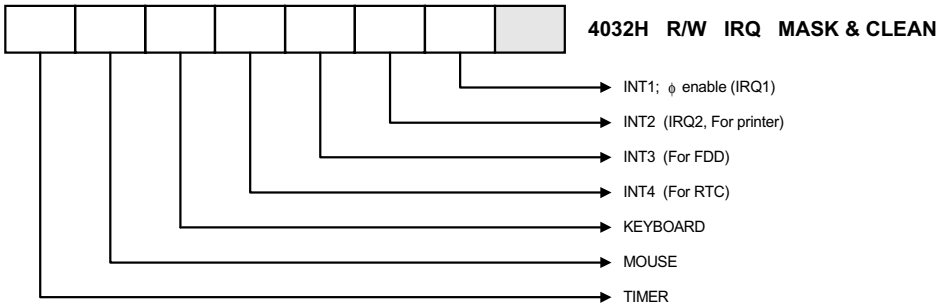
D7 - D0	**4014H W Source Address of Sprite's DMA**

This DMA is used for sprite only. The only way to renew sprite's data is by DMA. Writing this register will start DMA immediately. Normally, we continuously store new 256B data of sprite's parameter in working RAM. At V_Blank, makes data transfer by DMA. "D7-D0" of this register defines high byte address of CPU, which equals "A15-A8".

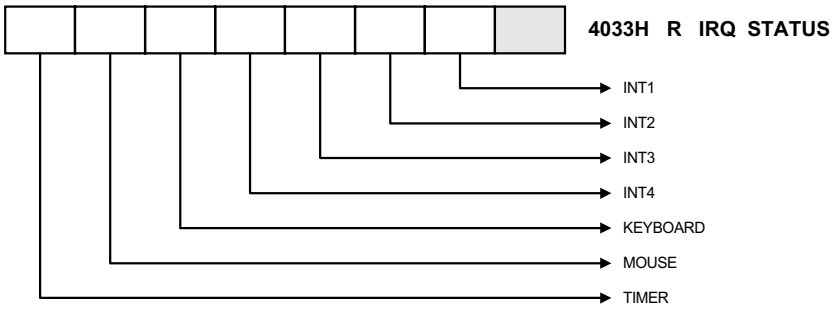
	L1 - L0	C3 - C0	**2040H - 207FH R/W Color Palette Table**

- C3 - C0 → Colors
- L1 - L0 → Luminance

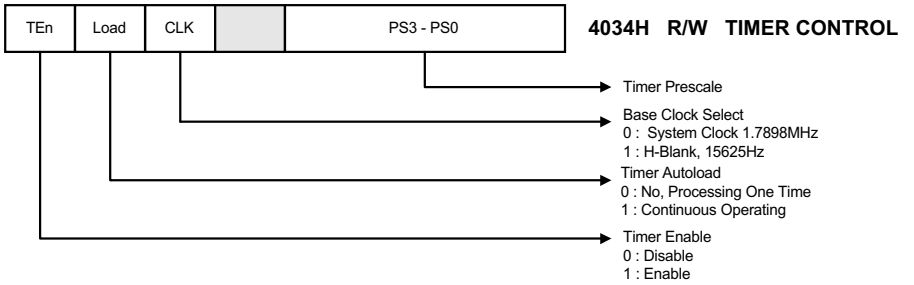
Color palette must be renewed during V_Blank or when GPU is off.



The IRQ-Mask relation bit is low active. If this bit is set to "0", then system will process an INT procedure when existing interrupted signal, and this status will store in IRQ status register. System can read from $4033 to check what kind of service is needed. If this bit is set to "1", the flag will clear and system will ignore the correlative interrupt.



The IRQ-Status relation bit is high active. Writing "1" of $4032 to clear flag when the INT routine has been finished.



TP7 - TP0	**4035H W TIMER PRESENT VALUE**
TC7 - TC0	**4036H R TIMER CURRENT VALUE**

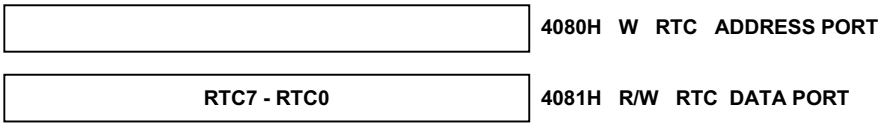
Select the system clock or H-Blank signal as a base clock source for a timer. The base clock will be divided by PS3-PS0, then clock will be connected to 8-bit counter (divided by this 8 bit counter again, current value). To select Base Clock from 1.7898MHz or 15625Hz, set the 4 bit prescaler and the 8 bit present down counter to obtain the timer's period from 3.84Hz to 1.7898MHz. The time period of timer is equal to the period of base clock multiplied by the pre-scale value and present value. (The calculation is shown below)

"Load" of $4034 sets the processing time of timer. If "Load" is set to "1", timer will process repeatedly until time is up, counter underflow. Thus, the CPU will receive a constant period of timer-IRQ. If "Load" is set to "0", timer will process down-count procedure one time, and one time for IRQ only. Time-Current-Value will be fixed at setting value.

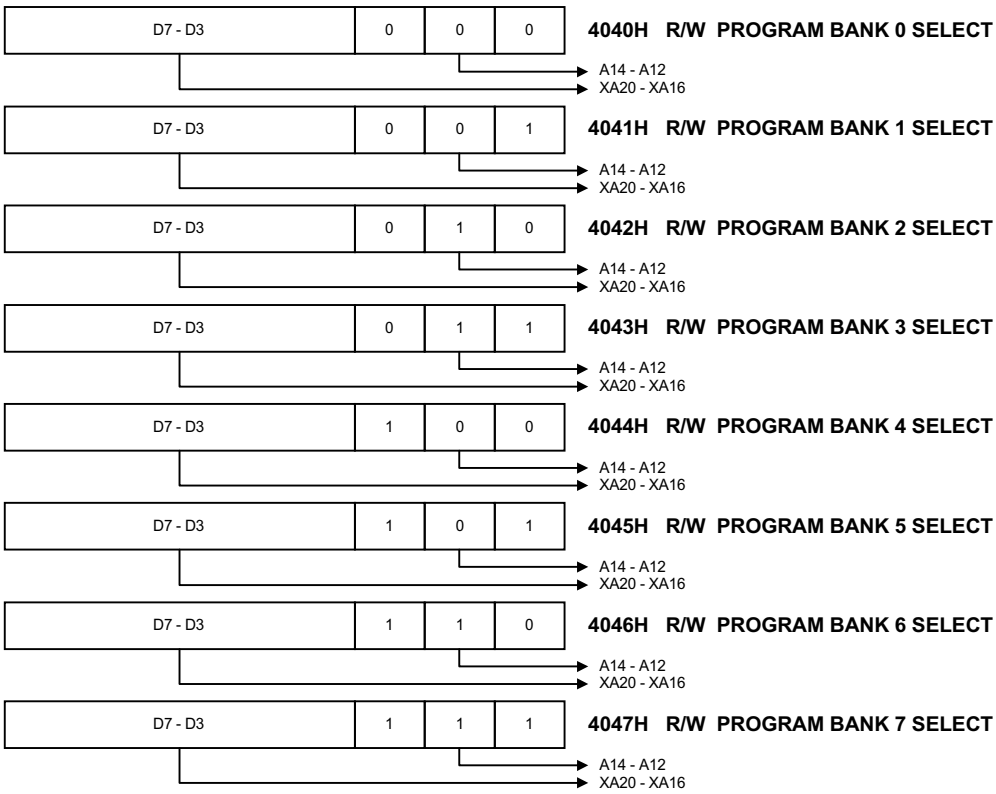
Time period of timer = period of base clock * (PS3 - PS0 +1) * (TP7 - TP0 +1)

Ex.: PS3 _ PS0 = 0FH
TP7 - TP0 = 3CH
Base clock = 15625Hz ($4034 - D5 = 0, = 64μs)
⇒ Time period = 64μs * (15 + 1) * (60 + 1)
= 62.46ms
= 16Hz

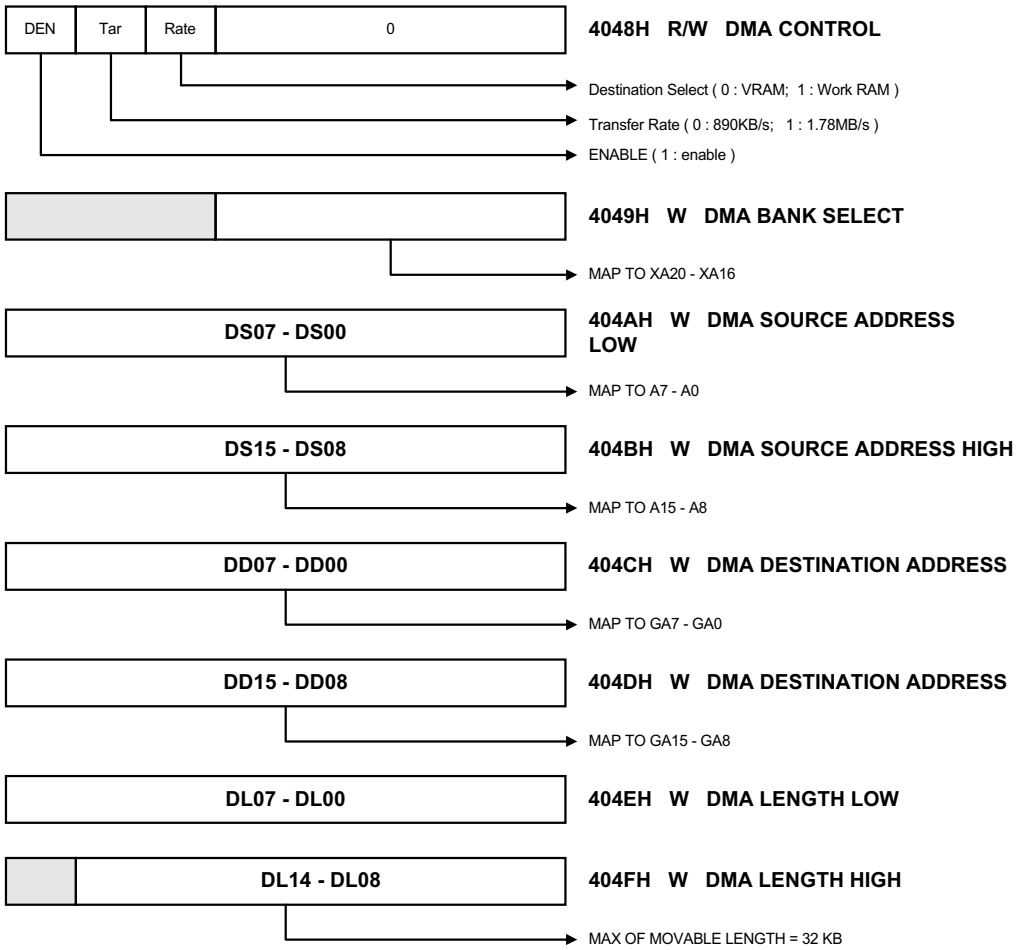
As writing data to Time-Present-Value register, data will be loaded into Time-Current-Value register at the same time. Then the down-count value of timer can be obtained by reading the Time-Current-Value register. Or system waits to receive an interrupt when time is up. Thus, this timer not only supplies a timer-interrupt function, but also functions as a current-timer.



SH6578 supports a RTC interface. When read/write data to RTC, the RTC address port must be set first then read or write data from/to the RTC data port.

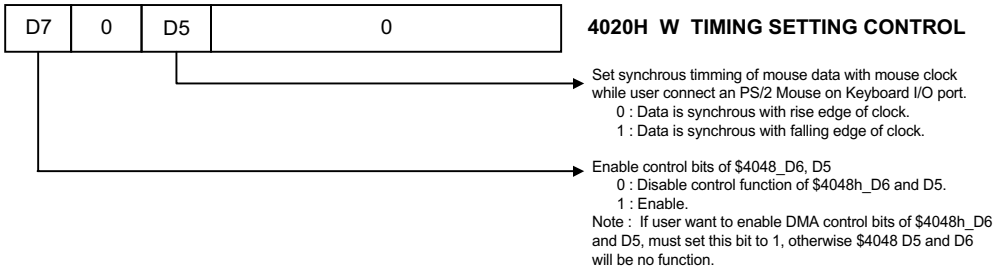


.
This function is used for expanding memory and dividing memory into small blocks. It works at $8000H - FFFFH only. (A15 equals to "1"). Setting 8 bits of data changes address mapping of CPU, D2 - D0 mapping to A14 - A12 & D7 - D3 mapping to XA20 - XA16. Each bank is defined as 4KB. User can set anyone bank at 1 MB memory space. The contents of above are the initial value which is constant at power on.
Changing the new address mapping replaces the original one.
Note: On application CKT, XA16 - XA20 of SH6578 are connected with A15 - A19 of ROM. So, the bank-select is taken as a continuous space changing.



Besides the DMA for Sprite RAM, SH6578 supports another DMA for the quick transformation of data from main memory to VRAM or working RAM. The source address of 1MB memory space is selected by setting DMA-Bank-Select & DMA-Source-Address register. The address of destination and source will increase by 1 automatically after moving 1 byte data.

As DMA transferring data to VRAM, processes only during V-Blank or PPU off, if DMA can't completely remove the data during a V_Blank period, the unfinished data will remain until next V_Blank period happens then the data will be continued to process automatically. As transferring data to working RAM, there is not limited as same as VRAM.



Note: This port is write only for enable the control function of DMA and clock synchronous mode for Keyboard communication, please remind 0 on the unused bit for default and refer to page 18 for more detail.

SD7 - SD0	41XX - 43XX R/W SUPER I/O ADDRESS

SH6578 has a super I/O (UM82C863) interface CKT which can connect with UM82C863 directly for extending functions of a floppy disk, printer, RS232, etc.

	D1	D0	4016H R/W JOYSTICK I/O PORT

	D0	4017H R JOYSTICK 2 /MOUSE PORT

Use the serial port to read data from joystick. Normally, there are 8 keys and an 8-bit shift register on the panel. Pre-load the key-data into the register first by $4016_D0 (OUT0) then read $4017 8 times.

```
Example:  reading Joystick 1
          LDA     #01
          STA     $4016          ; set OUT0 to "1" for pre-loading Key-data into register
          LDA     #00
          STA     #4016
          LDA     $4017          ; D0 is the first bit of key-PAD, and only "D0" is available.
          LDA     $4017          , D0 is the second bit of key-PAD, and only "D0" is available.
            :       :
            :       :
            :       :            ; 8 times
```

KBD7 - DBD0	4020H R KEYBOARD INPUT PORT W TIMMING SETTING CONTROL

Note: This port is read only for read the Keyboard data from Keyboard I/O, write data into this port will change some control functions, please refer to page 17 for more detail.

KBD7 - DBD0	4021H W KEYBOARD OUTPUT PORT

CLK	D6 - D3	DIR	0	DIR	4022H R/W KEYBOARD DATA CONTROL

SELECT DATA DIRECTION
0 : KEYBOARD > SYSTEM ; 1 : KEYBOARD < SYSTEM

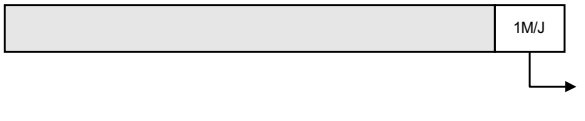
IRQ ENABLE FOR SENDING COMMAND
0 : DISABLE; 1 : ENABLE

SOFTWARE DRIVES SIGNAL OF KEYBOARD CLK DIRECTLY

During CPU sending command to Keyboard, if user enables the " IRQ Enable for Sending Command" bit, set to 1, that CPU will be informed that the data have been sent by an IRQ - same as keyboard IRQ. Then CPU can change the communication mode to receiving state. Otherwise, it is difficult to CPU to calculate the time of finished sending.

The AT compatible keyboard data is 11-bit stream. It contains start + scan code (8 bits) + parity + stop, totaling 11 bits. When hardware completely receives data, an interrupt will occur to inform the system to obtain this data. The scan code must be read before next keyboard data-bit in, otherwise, the following data will be lost.

The system also supports data communication between system and keyboard. The "DIR" signal defines the direction of transfer. As "DIR = 0", keyboard to system, system can get keyboard scan code by reading Keyboard-Input port at keyboard interrupt (internal). To send commands to keyboard, data must be written to "4021H" first, then set "DIR = 1" & "CLK = 0" a constant time (> 60ms). Finally, pull up "CLK = 1" signal. After "CLK" goes to high, the hardware CKT will transfer data to keyboard automatically.
* Note: In the RECEIVING mode, keyboard to system, user must set "CLK" to "1".



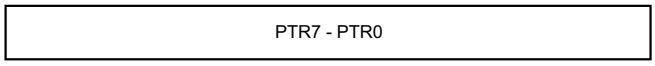
4023H R/W JOYSTICK/MOUSE CONTROL

4024H R MOUSE PORT
W MOUSE BAUD RATE SETTING

In this system, the signal of the joystick 2 and mouse are located at the same port; but user may only select one. First, the system must know the peripheral status, for example: connected joystick, mouse or other. Set/obtain information to/from these five registers (including 4016, 4017, and 4026). Set the joystick/mouse control, then send a reset (or preset) signal through "4026_D2". After reset, obtain information from the mouse port. If correct data is obtained, make sure that there is a mouse to be connected on this port. If not, follow the procedure of reading joystick data to get information.

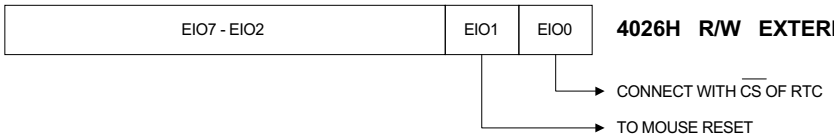
Note 1: The reset signal of mouse was connected with "4026_D2. Normally, reset time must be longer than 30ms. For detailed data of mouse, please refer to data format of MS mouse.

Note 2: Incurring to meeting the standard baud rate of mouse with different system clock of NTSC and PAL system. So needs to adjust the counter value of mouse controller though the Mouse Port ($4024h) with follow value.
#A3h: NTSC (default)
#A9h: PAL/B



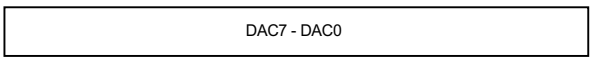
4025H W PRINTER PORT

SH6578 supports a simple function for printer. Writing data to this port will generate a strobe signal through PRT-ST to inform printer that the data is valid on the data bus. The printer will get data from data bus. Since the printer is an optional device, for getting printer status, paper end, etc., the user can use the extended I/O port to connect with printer.



4026H R/W EXTERNAL I/O PORT

This port contains 8 bits, all can be set as input/output. Each data line has a pull high resistor. On application CKT, EIO0 is used to control " $\overline{CS}$ " of RTC and EIO1 was used to generate reset signal to mouse. (For reference only)



4027H R/W DAC DATA REGISTER

System supports one 8-bit D/A converter for direct voice output. For voice function, use the timer to be a time base of the sampling rate and process voice data by software algorithm. (Like PCM, ADPCM)

Notes: 1. The waveform of voice has a DC bias(about 1/2 Vcc). The user must process bias by software(ramp up from "0" to 1/2 Vcc slowly) before voice output. Otherwise, a "pop" sound will be heard at the starting of the voice.
2. In order to be precise timing of voice output, the DAC has been designed to be synchronous with the timer. The actual timing of output is at timer-over flow. So must set timer while using DAC function.

PSG:

This system has built-in a 4-channel PSG (programmable Sound Generator). It can play 4 kinds of instrument sound simultaneous. The waveform of channel 1, 2 are square wave. Channel- 3's is a triangle wave, and channel 4 is a noise generator. For controlling timbre of channel 1& 2, there are envelop, duty of waveform, turn-on time, period repeat sound, pitch control and pitch-bend control, etc. can be programmable. Normally, these two channels are used for major melody channels. Channel 3 is suitable for some lower frequency instruments like BASE. Channel 4, noise channel, can make a special sound effect like base drum, snare drum, thunder and bomb sound by selecting bandwidth frequency and a suitable envelop.

PSG Port

Address	R/W	Signal Name	Register								Notes
			ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	
4000H	W	C1EC	IDY2	IDY1	1SC	1IW	1WI3	1WI2	1WI1	1WT0	Envelope Control
4001H	W	C1AT	1AT	1ST2	1ST1	1ST0	1SG	1AD2	1AD1	1AD0	Auto Tune Control
4002H	W	C1FT	1FT7	1FT6	1FT5	1FT4	1FT3	1FT2	1FT1	1FT0	Fine Tune Value
4003H	W	C1CT	1SL3	1SL2	1SL1	1SL0	1SL4	1FTA	1FT9	1FT8	Coarse Tune & Single Sound Control
4004H	W	C2EC	2DY2	2DY1	2SC	2IW	2WI3	2WI2	2WI1	2WI0	Envelope Control
4005H	W	C2AT	2AT	2ST2	2ST1	2ST0	2SG	2AD2	2AD1	2AD0	Auto Tune Control
4006H	W	C2FT	2FT7	2FT6	2FT5	2FT4	2FT3	2FT2	2FT1	2FT0	Fine Tune Value
4007H	W	C2CT	2SL3	2SL2	2SL1	2SL0	2SL4	2FTA	2FT9	2FT8	Coarse Tune & Single Sound Control
4008H	W	C3EN	3EN	3EL6	3EL5	3EL4	3EL3	3EL2	3EL1	3EL0	Single Sound Enable
400AH	W	C3FT	3FT7	3FT6	3FT5	3FT4	3FT3	3FT2	3FT1	3FT0	Fine Tune Value
400BH	W	C3CT	3SL3	3SL2	3SL1	3SL0	3SL4	3FTA	3FT9	3FT8	Coarse Tune & Single Sound Control
400CH	W	C4EC			4SC	4IW	4WI3	4WI2	4WI1	4WT0	Envelope Control
400EH	W	C4BF	4NS				4BF3	4BF2	4BF1	4BF0	Control Base Frequency
400FH	W	C4EN	4SL3	4SL2	4SL1	4SL1	4SL4				Channel Enable & Single Sound Control
4014H	W	DMADO	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	DMA High Byte Address
4015H	W	CHMK					C4EN	C3EN	C2EN	C1EN	Channel 1 - 4 Enable

PSG parameter description:

xDY2, xDY1: Waveform duty cycle of channel 1, 2. The output waveform of channel 1, 2 is square-wave which duty could be selected to 1/8, 1/4, 1/2 and 3/4.

0 0: 1/8 duty
0 1: 1/4 duty
1 0: 1/2 duty
1 1: 3/4 duty

xSC: Setting sound output of continuous period or 1 time only

0: single sound
1: continue

xIW: Envelop setting

0: A auto decay envelop is set which value from the highest value, Fh, decays to zero smoothly.
1: The envelop is kept on a constant level which set by xWI3 - xWI0.

xWI3 - xWI0: Envelop setting; If envelop is set to be a auto decay form, xIW = 0, xWIx set the slope of the envelope. The decay time from Fh to zero is
4.16mS X (xWI3 - xWI0).

If the envelop is set to be constant, xIW = 1, xWIx are used for setting envelop level. The value is equal to
Full scale X (xWI3 - xWI0)/15d

xAT: Sound effect control of pitch-band

1: enable; as enable, the frequency of this channel will smoothly shift from setting value to maximum or minimum frequency. That function is used for special sound effect, like machine gun. And the modulation rate of pitch band is set by xSTx.

xST2 - XST0: Setting the modulation time. Modulation time means the time of frequency change of each modulation. That is, the change rate is inverse-proportion to modulation time.

Modulation time = 8.33mS X (ST2 - ST0)

xSG: sign bit of xAD2 - xAD0

0: " + "
1: " - " negative

xAD2 - xAD0: Modulation value of frequency of each step

Fn+1 = Fn (1+ 2**-m) ; Means modulation frequency value is inverse-
m = xAD2 - xAD0 ; proportion to the value of "m".

xFTA - xFT0: Tone frequency setting

Frequency = 111,860 Hz/ (xFTA - xFT0), the minimum value of xFTA - xFT0 is 08H

xSL4 - xSL0: Sound duration of single sound

3EL6 - 3EL0: Turn on time of channel 3

Time = 4.16mS X (3EL6 - 3EL0)

3FTA - 3FT0: Tone frequency setting of channel 3

Frequency = 55,953 Hz/(3FTA - 3FT0)

4NS: Noise band of channel 4 setting

0: wide band
1: narrow band

xBF3 - xBF0: Select band width of channel 4

Absolute Maximum Ratings*

DC Supply Voltage V_{DD} - V_{SS} . . . . . .-0.3V to 7V

Input Voltage . . . . . GND -0.2V to V_{CC} +0.2V

Operating Temperature . . . . . .-10°C to +60°C

Storage Temperature . . . . . -50°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposed to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{CC} = 5V±5%, T_A = 0°C - 65°C, Loading = 30pF)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{CC}	Operating Voltage	4.75	5.0	5.25	V	
I_{DD}	Operating Current		60	90	mA	V_{CC} = 5V
V_{IH} V_{IL}	Input Voltage	2.4 0		Vcc 0.8	V	High Level Low Level
I1	Input Leakage		±25		µA	Tri_state Data bus
Ri	Input Resistor		200 6		KΩ KΩ	"Reset" pin & Normal pull high "Joy-stick" pin
V_{OH} V_{OL}	Output Voltage	2.4		0.6	V	I_{OH} = 4mA I_{OL} = -6mA
Vpp	Output Voltage		2.0 0.6		V	Video output, R_L = 20K Sound output, R_L = 1K

AC Characteristics (V_{CC} = 5V±5%, T_A = 0°C - 65°C, Loading = 30pF)

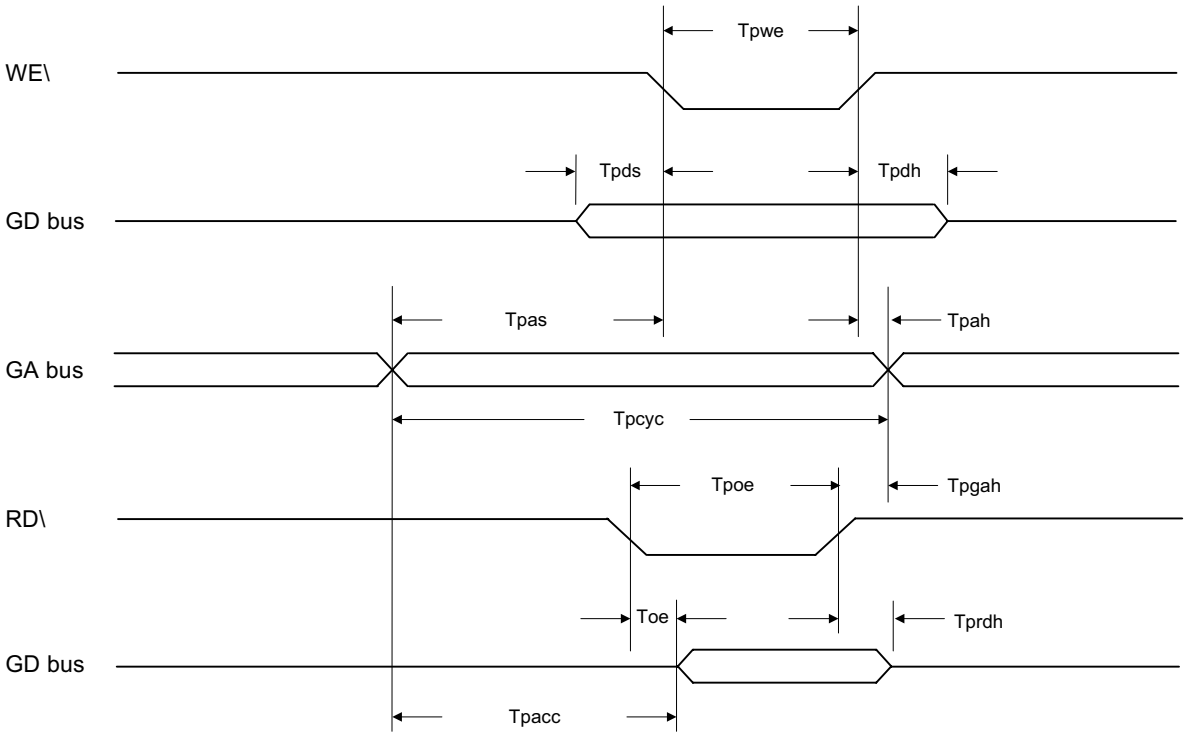
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Fosc	Input Clock		21.47727 26.6017125 21.453669 21.4923375		MHz	NTSC PAL-B PAL-M PAL-N
T02	ϕ2 cycle time		558 568		ns	NTSC PAL
Tphpw	ϕ2 high pulse width		349 319		ns	NTSC PAL
T1	ϕ2-ROM_CS\ delay time	10	25	40	ns	Loading = 20pF

AC Characteristics (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Trws	R/ W \ set-up time		60	90	ns	
Trwh	R/ W \ hold time	10	20		ns	
Tads	Address set-up time			90	ns	
Tadh	Address hold time	10			ns	
Tacc	Read data access time			200	ns	
Trds	Read data set-up time	50			ns	
Trdh	Read data hold time	10			ns	
Twds	Write data set-up time	100			ns	
Twdh	Write data hold time	20			ns	
Tpcyc	GA bus cycle time		372		ns	
Tpas	GA bus set-up time			50	ns	
Tpah	GA bus hold time	50			ns	
Tpds	GD bus set-up time	20			ns	
Tpdh	GD bus hold time	50			ns	
Tpwe	WE\ pulse width		186		ns	
Tpacc	Read GD bus access time			200	ns	
Toe	RD\-GD bus delay time			150	ns	
Tprdh	Read GD bus hold time	10			ns	
Tpoe	RD\ pulse width		200		ns	
Tpgah	RD\ GA bus hold time	20			ns	

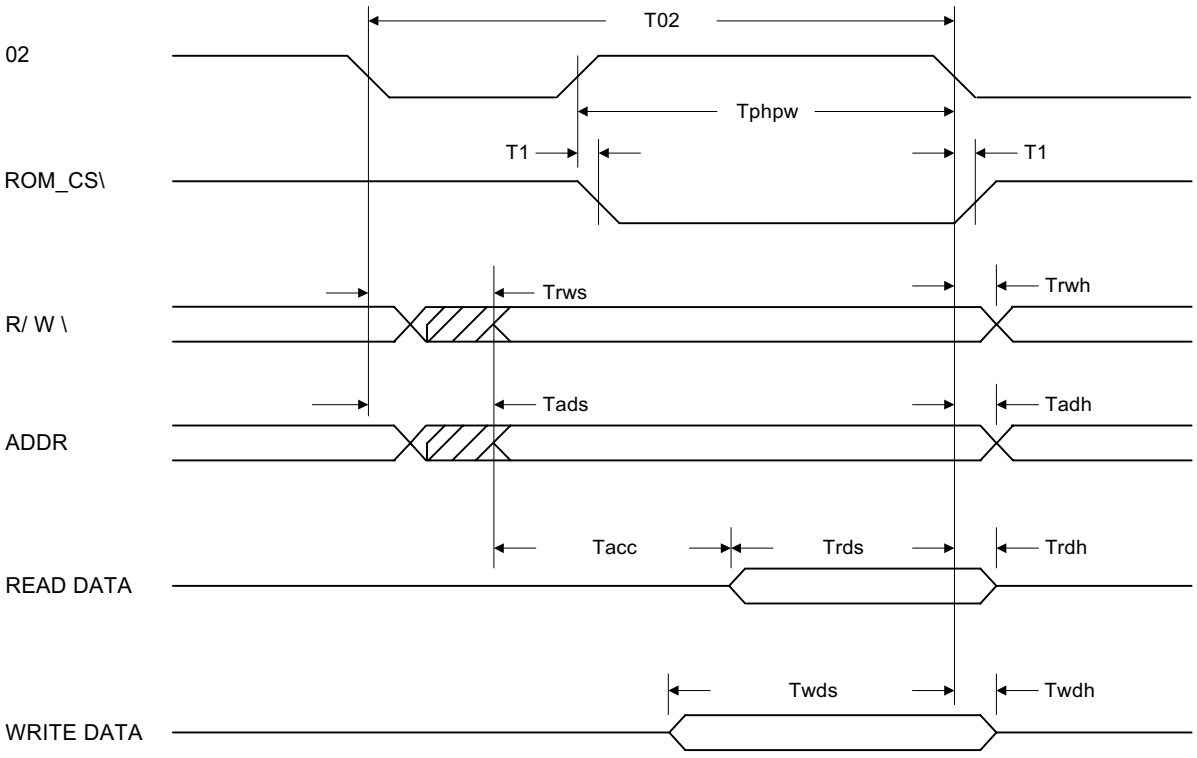
Timing Waveforms

Waveform Timing of Graphic Processor



Timing Waveforms (continued)

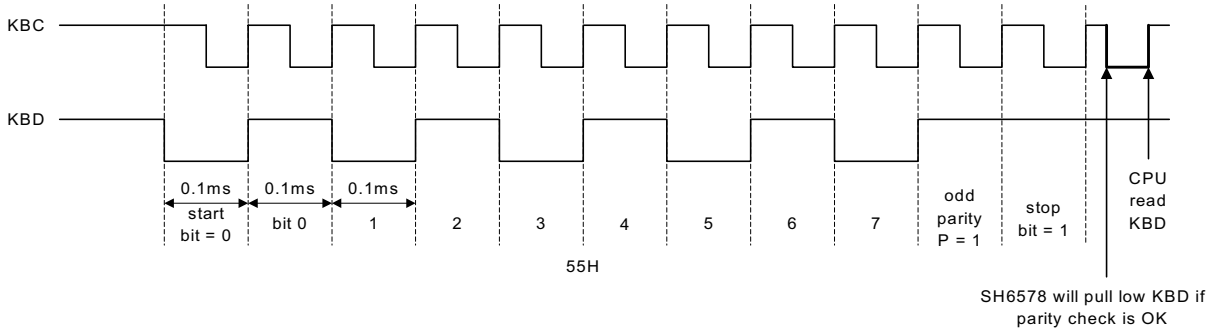
Waveform Timing of CPU Interface



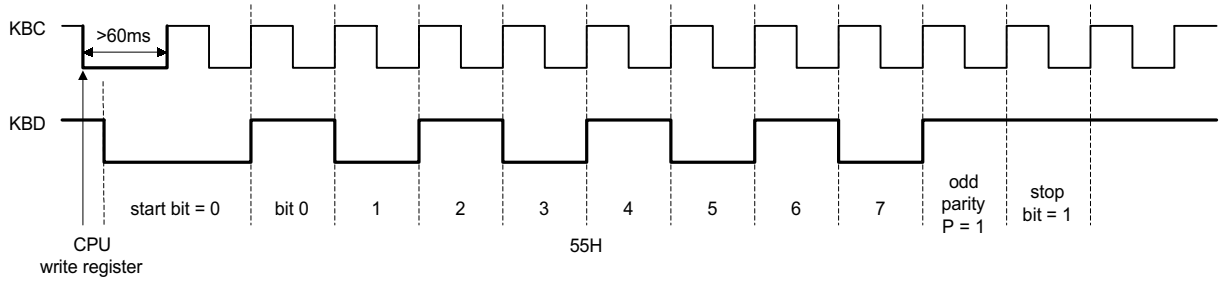
Timing Waveforms (continued)

Keyboard Interface Timing

A. Keyboard data input to SH6578



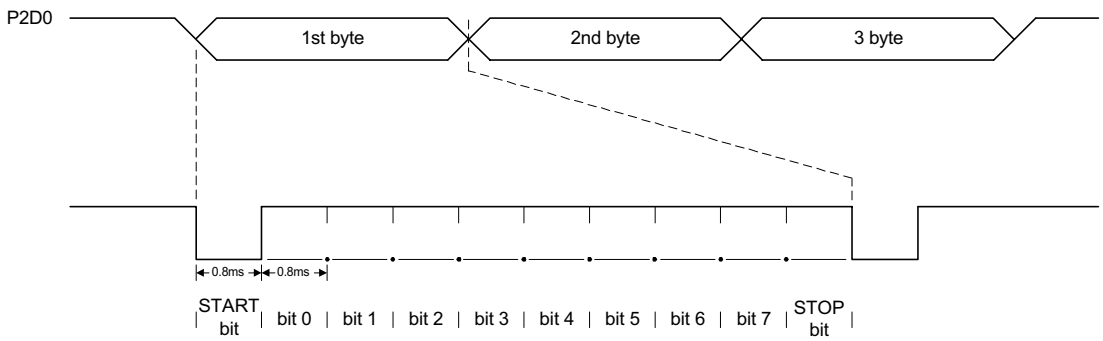
B. SH6578 Write Command to Keyboard



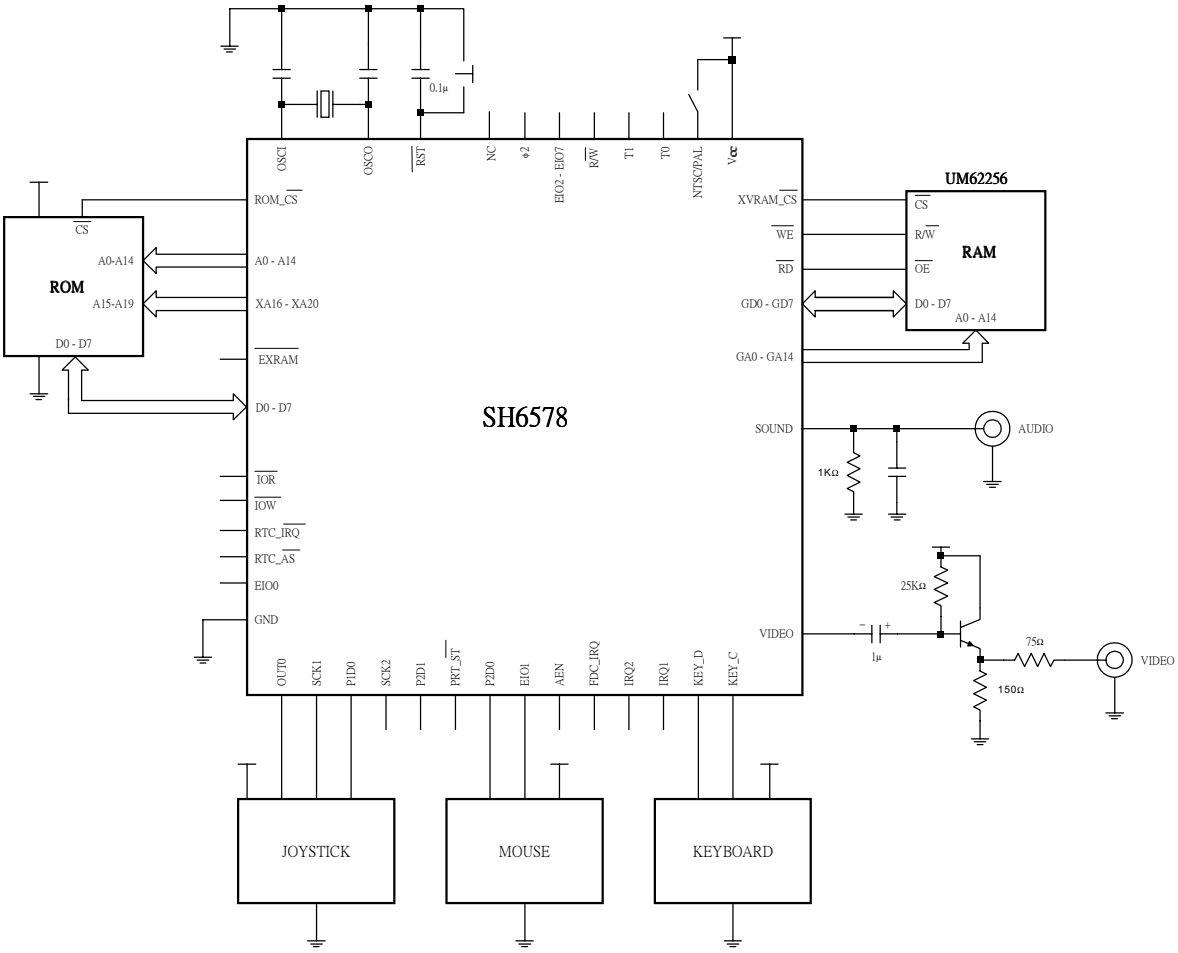
Mouse Interface Timing (MS mouse): mouse to SH6578

Output Byte Arrange

Bit No.	7	6	5	4	3	2	1	0
1st byte	X	1	L	R	V7	V6	H7	H6
2nd byte	X	0	H5	H4	H3	H2	H1	H0
3rd byte	X	0	V5	V4	V2	V2	V1	V0

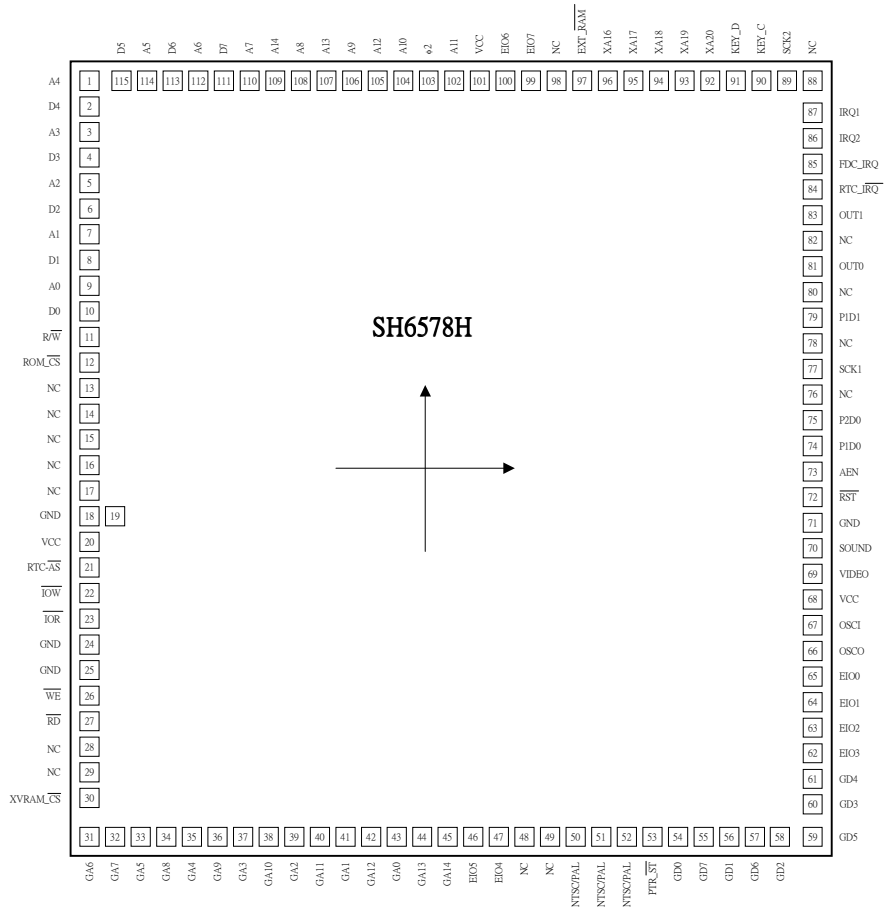


Application Circuit (for reference only)



* Note: UM62256 is optional device

Bonding Diagram



unit: mm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	A4	-2061	2076	11	R/ W	-2061	625
2	D4	-2061	1905	12	ROM_ CS	-2061	495
3	A3	-2061	1752	13	NC	-2061	365
4	D3	-2061	1599	14	NC	-2061	235
5	A2	-2061	1452	15	NC	-2061	105
6	D2	-2061	1312	16	NC	-2061	-26
7	A1	-2061	1171	17	NC	-2061	-156
8	D1	-2061	1031	18	GND	-2061	-286
9	A0	-2061	891	19	GND	-1926	-286
10	D0	-2061	755	20	VCC	-2061	-417

unit: mm

Pad No.	Designation	X	Y
21	RTC_$\overline{AS}$	-2061	-547
22	$\overline{IOW}$	-2061	-682
23	$\overline{IOR}$	-2061	-823
24	GND	-2061	-963
25	GND	-2061	-1104
26	$\overline{WE}$	-2061	-1244
27	$\overline{RD}$	-2061	-1391
28	NC	-2061	-1544
29	NC	-2061	-1697
30	XVRAM_$\overline{CS}$	-2061	-1850
31	GA6	-2061	-2076
32	GA7	-1890	-2076
33	GA5	-1737	-2076
34	GA8	-1584	-2076
35	GA4	-1437	-2076
36	GA9	-1297	-2076
37	GA3	-1156	-2076
38	GA10	-1016	-2076
39	GA2	-875	-2076
40	GA11	-735	-2076
41	GA1	-595	-2076
42	GA12	-454	-2076
43	GA0	-314	-2076
44	GA13	-173	-2076
45	GA14	-33	-2076
46	EIO5	106	-2076
47	EIO4	247	-2076
48	NC	387	-2076
49	NC	528	-2076
50	NTSC/PAL	668	-2076
51	NTSC/PAL	809	-2076
52	NTSC/PAL	949	-2076
53	PTR_$\overline{ST}$	1089	-2076
54	GD0	1230	-2076
55	GD7	1376	-2076
56	GD1	1529	-2076
57	GD6	1682	-2076
58	GD2	1835	-2076
59	GD5	2061	-2076
60	GD3	2061	-1905
61	GD4	2061	-1752
62	EIO3	2061	-1599
63	EIO2	2061	-1452
64	EIO1	2061	-1312
65	EIO0	2061	-1171
66	OSCO	2061	-1031
67	OSCI	2061	-891

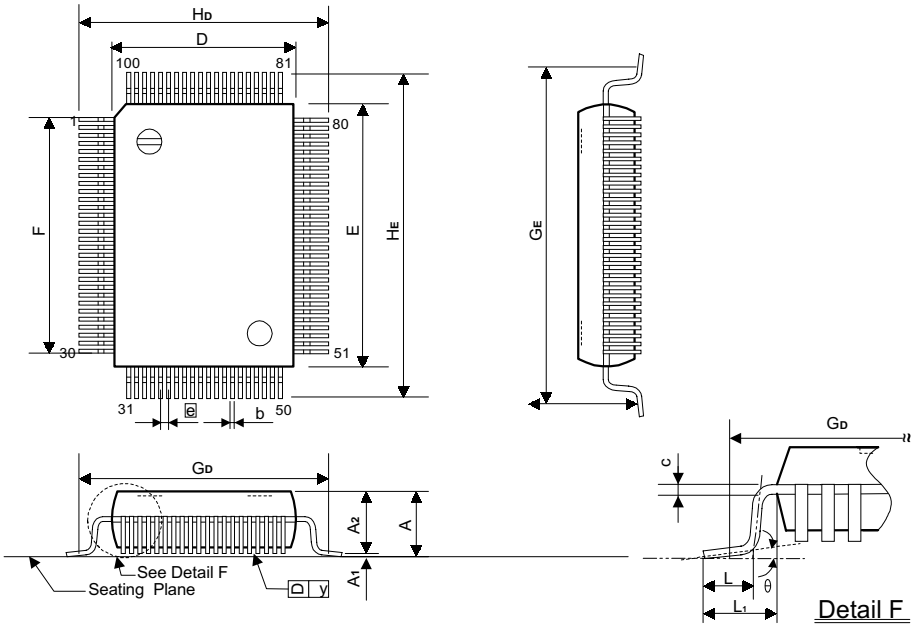
Pad No.	Designation	X	Y
68	VCC	2061	-755
69	VIDEO	2061	-625
70	SOUND	2061	-495
71	GND	2061	-364
72	$\overline{RST}$	2061	-234
73	AEN	2061	-104
74	P1D0	2061	26
75	P2D0	2061	156
76	NC	2061	286
77	SCK1	2061	417
78	NC	2061	547
79	P1D1	2061	682
80	NC	2061	823
81	OUT0	2061	963
82	NC	2061	1104
83	OUT1	2061	1244
84	RTC_$\overline{IRQ}$	2061	1391
85	FDC_IRQ	2061	1544
86	IRQ2	2061	1697
87	IRQ1	2061	1850
88	NC	2061	2076
89	SCK2	1890	2076
90	KEY_C	1737	2076
91	KEY_D	1584	2076
92	XA20	1437	2076
93	XA19	1297	2076
94	XA18	1156	2076
95	XA17	1016	2076
96	XA16	875	2076
97	EXT_$\overline{RAM}$	735	2076
98	NC	595	2076
99	EIO7	454	2076
100	EIO6	314	2076
101	VCC	173	2076
102	A11	33	2076
103	ϕ2	-106	2076
104	A10	-247	2076
105	A12	-387	2076
106	A9	-528	2076
107	A13	-668	2076
108	A8	-808	2076
109	A14	-949	2076
110	A7	-1089	2076
111	D7	-1230	2076
112	A6	-1376	2076
113	D6	-1529	2076
114	A5	-1682	2076
115	D5	-1835	2076

Ordering Information

Part No.	Package
SH6578F	100F QFP

Package Information

QFP 100L Outline Dimensions unit : inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.130 Max.	3.30 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.112±0.005	2.85±0.13
b	0.012 $^{+0.004}_{-0.002}$	0.31 $^{+0.10}_{-0.05}$
c	0.006 $^{+0.004}_{-0.002}$	0.15 $^{+0.10}_{-0.05}$
D	0.551±0.005	14.00±0.13
E	0.787±0.005	20.00±0.13
e	0.026 ±0.006	0.65±0.15
F	0.742 NOM.	18.85 NOM.
G_D	0.693 NOM.	17.60 NOM.
G_E	0.929 NOM.	23.60 NOM.
H_D	0.740±0.012	18.80±0.31
H_E	0.976±0.012	24.79±0.31
L	0.047±0.008	1.19±0.20
L_1	0.095±0.008	2.41±0.20
y	0.006 Max.	0.15 Max.
θ	0° ~ 12°	0° ~ 12°

Notes:
1. Dimensions D&E do not include resin fins.
2. Dimensions G_D & G_E are for PC Board surface mount pad pitch design reference only.